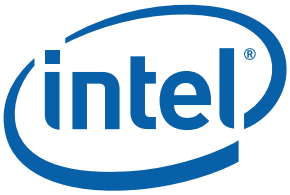


Intel® ME Firmware Integrated Clock Control (ICC) for Intel® Management Engine Firmware 8.0

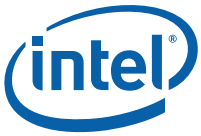
Tools User Guide

September 2011

Revision 0.8

Intel Confidential

Document Number: N/A



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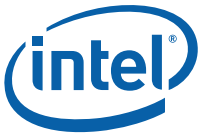


Revision History

Revision Number	Description	Revision Date
0.5	• Initial release	March 2011
0.6	• Added flags for WUOB command	May 2011
0.7	• Add new command gcem • Parameters changed for commands sl, sce, wuob and smr • Command capability changed for command smr • Remove temporary UOB in command gr • Update some examples in section 2.3 • Remove boot status errors "TempUobViolatedClkRangeLimits" and "TempUobApplyingFailure" in table 2.2 • Add one new CCT status message in section 2.4	June 2011
0.8	• Change Intel® 7 Series Express Chipset to Intel® 7 Series/C216 Chipset Family	September 2011

1 Introduction

The purpose of the document is to provide guidance on the usage of the tools provided for Integrated Clock Control (ICC) included within the Intel® Management Engine (Intel® ME) firmware kit.

1.1 Terminology

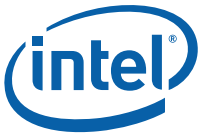
Table 1-1. Terminology

Acronym or Term	Definition
API	Application Programming Interface
BIOS	Basic Input Output System
CCT	Clock Commander Tool
CCTwin	Windows* command line version of the Clock Commander Tool
CPU	Central Processing Unit
DLL	Dynamic Link Library
FITC	Flash Image Tool
FW	Firmware
HECI (deprecated)	Host Embedded Controller Interface
ICC	Integrated Clock Control
Intel® ME	Intel Management Engine
Intel® MEI	Intel Management Engine Interface (formerly HECI)
PCH	Platform Controller Hub
Permanent UOB	UOB that is applied on every boot.
UOB	Update on Boot. An record of ICC registers setting that are applied on the next platform boot.

1.2 Reference Documents

Table 1-2. Reference Documents

Document	Document No. / Location
Intel® 7 Series/C216 Chipset Family SPI Programming Guide	FW release kit
Intel® 7 Series/C216 Chipset Family Intel® Management Engine Firmware Bring Up Guide	FW release kit
Intel® 7 Series/C216 Chipset Familiy Platform Controller Hub (PCH) External Design Specification (EDS)	Please contact your FAE for availability.



2 ICC Tools

This document covers the usage of the Clock Commander Tool (CCT) included in the ..\Tools\ICC_tools\ directory. Details on other tools can be found in the tools user guides included in the other tools directories contained within the firmware kit.

The CCT tools included in the Intel® 7 Series/C216 Chipset Family firmware release kit are designed for Intel® 7 Series/C216 Chipset Family based platforms only. These tools will not function on other legacy platforms.

2.1 Command Line Interface

CCT.exe and CCTwin.exe support the following command line options. To view all of the supported options, run the application with no arguments or with the ? option. The command syntax for the CCT tool is CCT [options] command [arguments].

The Windows* version of the tool - CCTwin.exe - requires that the Intel MEI driver is loaded for it to function.

The available options are:

/v0 - verbose level 0. This is the default mode and provides the smallest amount of information.

/v1 - verbose level 1. This is the debug mode and includes additional debug information including the raw Intel MEI message information.

The available CCT command are:

CCT	gcc [no arguments]
	gcdr [selector] [OEM index]
	gl [no arguments]
	sl [registers to lock] [params]
	sce [clock enables] [clock enables mask] [params]
	gp [no arguments]
	sp [profile number]
	gr [selector]
	rr [buffered[1] register or registers to read]
	rrd [buffered[1]]
	wr [register offset] = [register value]
	wuob [flags] [register offset] = [register value]
	gcem [params]
	smr [buffered[1]] [register to read]
	smw [register offset or name] = [register value]

NOTES:
1. Optional for registers that have two stages. The buffered option is for reading the first stage value.

gcc
Gets ICC clock capabilities

gcdr
Gets combined clock range definition record used by FW. Could be run with “oem” selector. If so then requested clock range definition record for current profile is returned. If a record index is specified (e.g. oem 1) then requested clock range definition record for profile #1 is returned.

gl
Show which registers are locked and cannot be written after EOP.

sl
Locks specified registers. The registers to be locked can be specified as symbolic names or as 32 bit register masks. A single register can be specified or a list of registers can be specified. This command would typically be used by BIOS developers. This command is to specify which registers will be unlocked/locked after EOP. This command will not work after the BIOS sends the End of Post Intel MEI message. A flag option “noresp” can be used if CCT doesn’t want a response from ME FW.

sce
Enables or disables selected PCI clock outputs. The clock enables argument is a 32 bit value which specifies the clock output settings. The clock enables mask argument is a 32 bit value which specifies which clock outputs will be enabled or disabled. This command would typically be used by BIOS developers. This command will not work after the BIOS sends the End of Post Intel MEI message. A flag option “noresp” can be used if CCT doesn’t want a response from ME FW.

gp
Gets the currently used ICC profile number.

sp
Sets the ICC profile to the number specified in the profile number argument. This command will not work after the BIOS sends the End of Post Intel MEI message.

gr
Gets the ICC record specified in the selector argument. The available selectors are:
intel - Intel record
oem - OEM record
perm - permanent UOB record
preuob - platform boot time record pre UOB
postuob - platform boot time record post UOB
current - current record

rr
Reads registers based on the register argument. The register can be specified as a list of decimal or hexadecimal offsets or a list of symbolic names. When specified as a list offsets and symbolic names can be mixed. Registers can also be specified as a range in which case only numbers can be used. This command also accepts the buffered option for registers that have two stages.

rrd
This command takes no arguments and returns the values for all of the dynamic ICC registers. This command also accepts the buffered option for registers that have two stages.

wr
This command writes ICC registers based on the register offset and value arguments. The arguments need to be specified in the form of a pair in the form of *register offset* = *register value*. the register offset can be specified as a number or as a symbolic name.

wuob
Write a UOB record. The flag for this command is invalid - invalidation request for the UOB record. If no flags are used, a permanent UOB is created or invalidated.

gcem
Get currently used clock enables mask set in SPI image by OEM. An optional index parameter could be used for the given ICC profile.

smr
SMBus register read. Reads a single ICC register via SMBus. This command is only present in CCTwin.exe.

smw
SMBus register write. Writes a single ICC register via SMBus. This command is only present in CCTwin.exe.

2.2 SMBus Commands and Setup

The Windows* version of the Clock Commander Tool supports two SMBus commands - smr and smw. These commands require a host or control system with the Aardvark* SMBus analyzer installed and the Aardvark.dll. The cct.ini file also needs to be present in the same directory as cctwin.exe. The cct.ini file needs to contain the correct SMBus settings that match the settings for the flash image on the system under test.

Smr and smw are the only commands that are supported over the SMBus.

2.2.1 Software Components

The software components on the host system that are required for the Clock Commander Tool SMBus commands to function are:

- cctwin.exe; available in the Intel ME FW kit
- cct.ini; available in the Intel ME FW kit
- Aardvark.dll; available at http://www.totalphase.com/products/aardvark_i2cspi/(tab Downloads | Aardvark Software and API library for Windows - Use aardvark.dll from ‘net’ directory in the zip file
- Aardvark USB driver; Available on www.totalphase.com or installation CD that came with the Aardvark. Link http://www.totalphase.com/products/aardvark_i2cspi/(tab Downloads | USB Drivers)

2.2.1.1 Installation

- Copy cctwin.exe and cct.ini to a directory on the host system
- Install the latest drivers for the Aardvark host adapter onto the host system
- Download the Aardvark.dll file from Total Phase*. The Aardvark.dll file needs to be placed into one of the following folders on the host system:
  - Directory of cctwin.exe
  - Any directory within the PATH environment variable

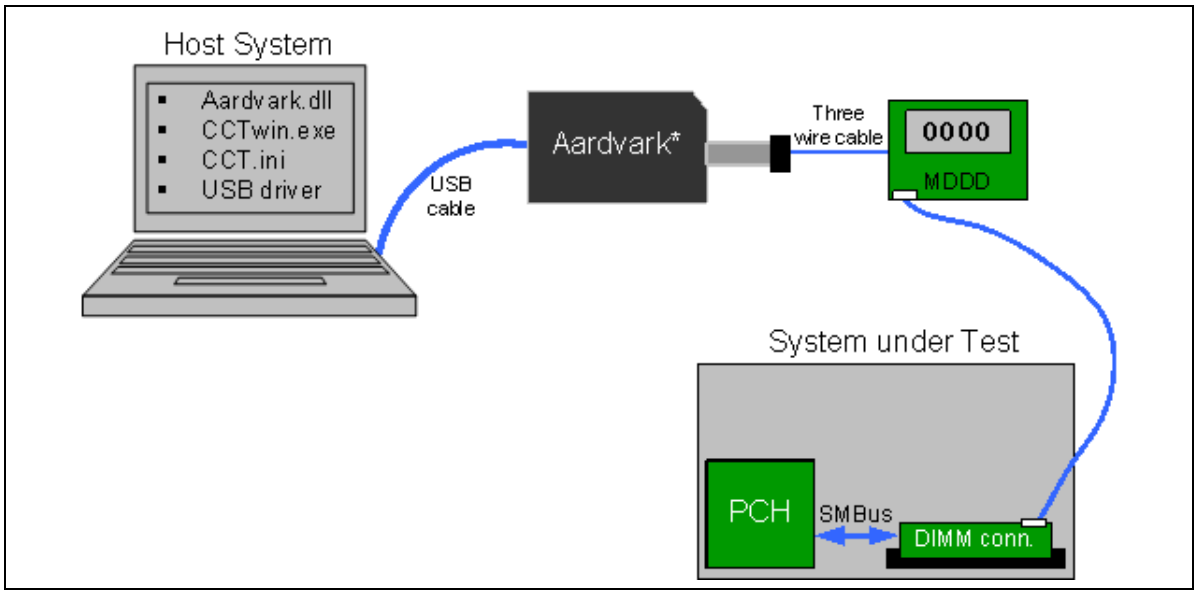
2.2.2 Hardware Components

Usage of the Clock Commander Tool SMBus commands requires a connection to the SMBus. This can be accomplished with an Aardvark* I2C/SPI Host Adapter (Part Number TP240141) manufactured by Total Phase* Inc (http://www.totalphase.com/products/aardvark_i2cspi/).

Connection of the Aardvark* to the SMBus interface of the system under test can be accomplished in two ways:

- Use MDDD to access the SMBus signals through the DIMM slot. See Figure 2-1.
- Directly connect the Aardvark to the SMBus signals CLK, DATA, GND on the system under test

Figure 2-1. Connecting Aardvark* via MDDD

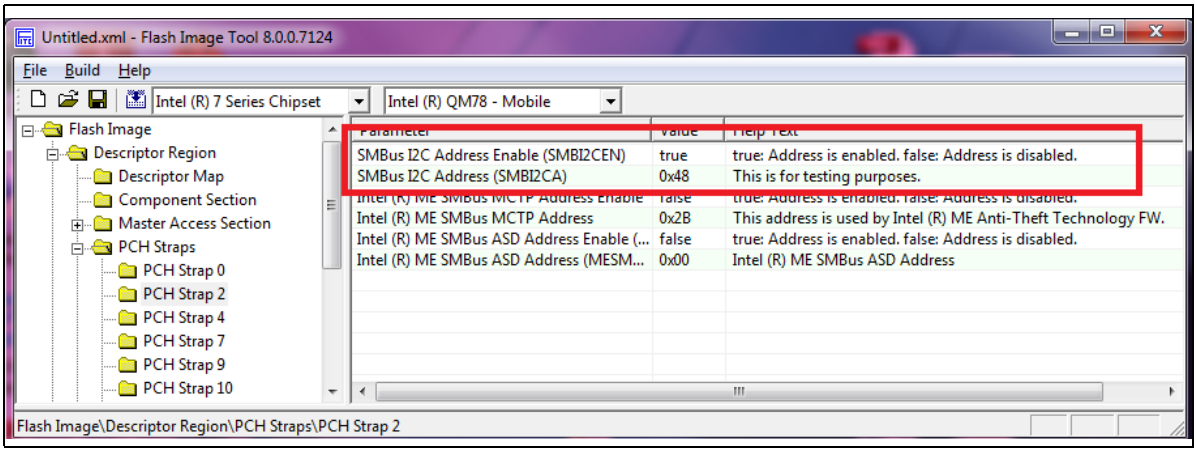


2.2.3 Softstrap Settings in FITC

When building an image with FITC, the following settings are required to use the SMBus commands available in cctwin.exe:

- PCH Strap 0 Intel ME SMBus Enable set to True
- PCH Strap 2 SMBus I2C Enable (SMBI2CEN) set to True
- SMBus I2C Address (SMBI2CA) set to 0x48. Other addresses are not supported.

Figure 2-2. Enabling CCT SMBus Register Access in FITC



2.2.4 Cct.ini File Settings

In order for the cctwin.exe SMBus commands to work properly the cct.ini file needs to be present in the same directory as cctwin.exe. The settings in the cct.ini file need to match the settings in the flash image of the system under test. The default settings of the cct.ini file are:

```
[smbus]
host_addr = 0x37 ; address of the CCT host
fw_addr   = 0x48 ; address of the Firmware client
baudrate  = 100  ; kHz
timeout   = 200  ; ms
```

The fw_addr field should match the setting for the SMBus I2C Address (SMBI2CA) as configured in FITC. The baudrate and timeout settings should not be changed from the default values. The host_addr setting is the SMBus address for the control or host system. If there is an address conflict on the host system, this value can be changed.

2.3 Examples

2.3.1 Example 1 - Get Clock Capabilities

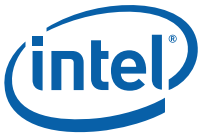
```
C:\cct>cctwin.exe gcc
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

icc_hw_version_number = 0002.0000
icc_hw_sku = ENHANCED
icc_boot_status_report [0x02400000]:
     boot event: "SetClockEnablesReceived"
     boot event: "IntelCRDRSkuReduceEnhancedUpperRange"


HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.2 Example 2 - Get Intel Clock Range Definition Record

```
C:\cct>cctwin.exe gcdr intel
```




```
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.


clock_id = 1[DIV1-S]

clock_usage = {} -> NOT USED
frequency_min                          = 38.0952 MHz
frequency_max                          = 800.0000 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 1
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 2.50 %

clock_id = 2[DIV2-S]

clock_usage = {} -> NOT USED
frequency_min                          = 38.0952 MHz
frequency_max                          = 800.0000 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 1
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 2.50 %

clock_id = 3[DIV3]

clock_usage = {} -> NOT USED
frequency_min                          = 99.5463 MHz
frequency_max                          = 100.0000 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 0.50 %

clock_id = 4[DIV4]

clock_usage = {} -> NOT USED
frequency_min                          = 38.0952 MHz
frequency_max                          = 800.0000 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 1
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 2.50 %

clock_id = 5[DIV1-NS]

clock_usage = {} -> NOT USED
frequency_min                          = 120.0000 MHz
frequency_max                          = 120.0000 MHz
ssc_change_allowed                     = 0
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
```

```
ssc_spread_mode_control_down_allowed   = 0
ssc_spread_percent_max                 = 0.00 %

clock_id = 6[DIV2-NS]

clock_usage = {} -> NOT USED
frequency_min                          = 100.0000 MHz
frequency_max                          = 100.0000 MHz
ssc_change_allowed                     = 0
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 0
ssc_spread_percent_max                 = 0.00 %


HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.3 Example 3 - Get OEM Clock Range Definition Record

```
C:\cct>cctwin.exe gcdr OEM 0
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.


clock_id = 1[DIV1-S]

clock_usage = {Display}
frequency_min                          = 120.0000 MHz
frequency_max                          = 120.0000 MHz
ssc_change_allowed                     = 0
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 0.50 %

clock_id = 2[DIV2-S]

clock_usage = {BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3}
frequency_min                          = 100.0000 MHz
frequency_max                          = 100.0000 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 0.50 %

clock_id = 3[DIV3]

clock_usage = {} -> NOT USED
frequency_min                          = 100.0000 MHz
frequency_max                          = 100.0000 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 0.50 %
```

```
clock_id = 4[DIV4]

clock_usage = {Display_Bending}
frequency_min                          = 119.3473 MHz
frequency_max                          = 120.6599 MHz
ssc_change_allowed                     = 1
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 1
ssc_spread_mode_control_down_allowed   = 1
ssc_spread_percent_max                 = 2.50 %

clock_id = 5[DIV1-NS]

clock_usage = {Display}
frequency_min                          = 120.0000 MHz
frequency_max                          = 120.0000 MHz
ssc_change_allowed                     = 0
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 0
ssc_spread_percent_max                 = 0.00 %

clock_id = 6[DIV2-NS]

clock_usage = {BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3}
frequency_min                          = 100.0000 MHz
frequency_max                          = 100.0000 MHz
ssc_change_allowed                     = 0
ssc_spread_mode_control_up_allowed     = 0
ssc_spread_mode_control_center_allowed = 0
ssc_spread_mode_control_down_allowed   = 0
ssc_spread_percent_max                 = 0.00 %


HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.4 Example 4 - Get Lock

```
C:\cct>cctwin.exe gl
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

[0x00] CSS                -> LOCKED
[0x01] SSS                -> LOCKED
[0x02] FCSS               -> LOCKED
[0x03] PLLRCS             -> LOCKED
[0x04] ---                -> LOCKED
[0x05] ---                -> LOCKED
[0x06] ---                -> LOCKED
[0x07] ---                -> LOCKED
[0x08] ---                -> LOCKED
[0x09] ---                -> LOCKED
[0x0a] ---                -> LOCKED
[0x0b] ---                -> LOCKED
[0x0c] PLLEN              -> LOCKED
```

```
[0x0d] ---              -> LOCKED
[0x0e] OCKEN            -> LOCKED
[0x0f] IBEN             -> LOCKED
[0x10] DIVEN            -> LOCKED
[0x11] ---              -> LOCKED
[0x12] PM1              -> LOCKED
[0x13] PM2              -> LOCKED
[0x14] ---              -> LOCKED
[0x15] ---              -> LOCKED
[0x16] ---              -> LOCKED
[0x17] ---              -> LOCKED
[0x18] ---              -> LOCKED
[0x19] ---              -> LOCKED
[0x1a] ---              -> LOCKED
[0x1b] ---              -> LOCKED
[0x1c] SEBP1            -> LOCKED
[0x1d] SEBP2            -> LOCKED
[0x1e] ---              -> LOCKED
[0x1f] ---              -> LOCKED
[0x20] DIVSET           -> UNLOCKED
[0x21] ---              -> UNLOCKED
[0x22] ---              -> LOCKED
[0x23] ---              -> LOCKED
[0x24] SSCCTL           -> UNLOCKED
[0x25] ---              -> LOCKED
[0x26] ---              -> LOCKED
[0x27] ---              -> LOCKED
[0x28] ---              -> LOCKED
[0x29] PI12BiasParms    -> LOCKED
[0x2a] ---              -> LOCKED
[0x2b] ---              -> LOCKED
[0x2c] ---              -> LOCKED
[0x2d] ---              -> LOCKED
[0x2e] ---              -> LOCKED
[0x2f] ---              -> LOCKED
[0x30] SSC1PARMS        -> UNLOCKED
[0x31] SSC2PARMS        -> UNLOCKED
[0x32] SSC3PARMS        -> UNLOCKED
[0x33] SSC4PARMS        -> UNLOCKED
[0x34] ---              -> LOCKED
[0x35] ---              -> LOCKED
[0x36] ---              -> LOCKED
[0x37] ---              -> LOCKED
[0x38] ---              -> UNLOCKED
[0x39] SSC2OCPARMS      -> UNLOCKED
[0x3a] ---              -> UNLOCKED
[0x3b] ---              -> UNLOCKED
[0x3c] ---              -> LOCKED
[0x3d] ---              -> LOCKED
[0x3e] ---              -> LOCKED
[0x3f] ---              -> LOCKED
[0x40] ---              -> LOCKED
[0x41] ---              -> LOCKED
[0x42] ---              -> LOCKED
[0x43] ---              -> LOCKED
[0x44] ---              -> LOCKED
```

```
[0x45] ---                -> LOCKED
[0x46] ---                -> LOCKED
[0x47] ---                -> LOCKED
[0x48] PMSRCCLK1          -> LOCKED
[0x49] PMSRCCLK2          -> LOCKED
[0x4a] ---                -> LOCKED
[0x4b] ---                -> LOCKED
[0x4c] ---                -> LOCKED
[0x4d] ---                -> LOCKED
[0x4e] ---                -> LOCKED
[0x4f] ---                -> LOCKED
[0x50] ---                -> LOCKED
[0x51] ---                -> LOCKED
[0x52] ---                -> LOCKED

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.5 Example 5 - Get Profiles

```
C:\cct>cctwin.exe gp
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

number_of_icc_profiles          = 4
oem_boot_profile_number         = 0
icc_profile_is_selected_by      = oem (strap)
current_boot_profile_index      = 0

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.6 Example 6 - Get Record (Intel)

```
C:\cct>cctwin.exe gr intel
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

FLAGS [0x00012048]
record_length                     = 72

REGISTERS
[0x00] CSS                = 0x00011a33
[0x02] FCSS               = 0x00000232
[0x03] PLLRCS             = 0x00088cbf
[0x0c] PLLEN              = 0x0000000c
[0x10] DIVEN              = 0x000005eb
[0x12] PM1                = 0x0000001f
[0x18] ---                = 0x0e11175d
[0x20] DIVSET             = 0x00455551
[0x24] SSCCTL             = 0x00010000
[0x2b] ---                = 0x000087c0
[0x2e] ---                = 0x15780001
[0x32] SSC3PARMS          = 0x12704c30
[0x33] SSC4PARMS          = 0x1270a428
[0x3b] ---                = 0x00000100

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.7 Example 7 - Get Record (Current)

```
C:\cct>cctwin.exe gr current
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

FLAGS [0x000120d8]
record_length                    = 216

REGISTERS
[0x00] CSS               = 0x00011a33[LOCKED]
[0x01] SSS               = 0x00033733[LOCKED]
[0x02] FCSS              = 0x00000232[LOCKED]
[0x03] PLLRCS            = 0x00088cbf[LOCKED]
[0x04] ---               = 0x00030e08[LOCKED]
[0x08] ---               = 0x00030e08[LOCKED]
[0x09] ---               = 0x00008000[LOCKED]
[0x0b] ---               = 0x00000080[LOCKED]
[0x0c] PLLEN             = 0x6000000c[LOCKED]
[0x0d] ---               = 0x0f1ff1ff[LOCKED]
[0x0e] OCKEN             = 0x1fde078f[LOCKED]
[0x0f] IBEN              = 0x0000002f[LOCKED]
[0x10] DIVEN             = 0x000005eb[LOCKED]
[0x12] PM1               = 0x0000001f[LOCKED]
[0x13] PM2               = 0x00000000[LOCKED]
[0x14] ---               = 0x00fbfbfb[LOCKED]
[0x15] ---               = 0x0000fbfb[LOCKED]
[0x16] ---               = 0x000000ff[LOCKED]
[0x17] ---               = 0xbbbbbbbb[LOCKED]
[0x18] ---               = 0x0000175d[LOCKED]
[0x19] ---               = 0x00000834[LOCKED]
[0x1c] SEBP1             = 0x00009999[LOCKED]
[0x1d] SEBP2             = 0x00099999[LOCKED]
[0x1e] ---               = 0x00000000[LOCKED]
[0x20] DIVSET            = 0x0054f551[UNLOCKED]
[0x21] ---               = 0x00000551[UNLOCKED]
[0x24] SSCCTL            = 0x00010000[UNLOCKED]
[0x27] ---               = 0x00000020[LOCKED]
[0x28] ---               = 0x00640004[LOCKED]
[0x29] PI12BiasParms     = 0x08880888[LOCKED]
[0x2a] ---               = 0x08880888[LOCKED]
[0x2b] ---               = 0x000087c0[LOCKED]
[0x2c] ---               = 0x00000000[LOCKED]
[0x2d] ---               = 0x00000000[LOCKED]
[0x2e] ---               = 0x15780001[LOCKED]
[0x2f] ---               = 0x00000001[LOCKED]
[0x30] SSC1PARMS         = 0x1270a428[UNLOCKED]
[0x31] SSC2PARMS         = 0x12704c30[UNLOCKED]
[0x32] SSC3PARMS         = 0x12704c30[UNLOCKED]
[0x33] SSC4PARMS         = 0x1270a428[UNLOCKED]
[0x38] ---               = 0x00000000[UNLOCKED]
[0x39] SSC2OCPARMS       = 0x00000000[UNLOCKED]
[0x3a] ---               = 0x00000000[UNLOCKED]
[0x3b] ---               = 0x00000000[UNLOCKED]
[0x40] ---               = 0x29c529c5[LOCKED]
[0x41] ---               = 0x29c529c5[LOCKED]
```

```
[0x48] PMSRCCLK1          = 0x76543210[LOCKED]
[0x49] PMSRCCLK2          = 0x00000f98[LOCKED]
[0x4d] ---                = 0x00000002[LOCKED]
[0x4f] ---                = 0x00000000[LOCKED]

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.8 Example 8 - Get Record (Permanent)

```
C:\cct>cctwin.exe gr perm
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

FLAGS [0x00006004]
record_length                    = 4
temporary                        = 0
registers_section_does_not_exist  = 1
valid                            = 0

invalidate_reason: "Power Loss"


HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.9 Example 9 - Read Register (All)

```
C:\cct>cctwin.exe rr 0x00:0x52
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

[0x00] CSS                = 0x00011a33
[0x01] SSS                = 0x00033733
[0x02] FCSS               = 0x00000232
[0x03] PLLRCS             = 0x00088cbf
[0x04] ---                = 0x00030e08
[0x05] ---                = 0x00840121
[0x06] ---                = 0x00840121
[0x07] ---                = 0x00840121
[0x08] ---                = 0x00030e08
[0x09] ---                = 0x00008000
[0x0a] ---                = 0x00840121
[0x0b] ---                = 0x00000080
[0x0c] PLLEN              = 0x6000000c
[0x0d] ---                = 0x0f1ff1ff
[0x0e] OCKEN              = 0x1fde078f
[0x0f] IBEN               = 0x0000002f
[0x10] DIVEN              = 0x000005eb
[0x11] ---                = 0x00840121
[0x12] PM1                = 0x0000001f
[0x13] PM2                = 0x00000000
[0x14] ---                = 0x00fbfbfb
[0x15] ---                = 0x0000fbfb
[0x16] ---                = 0x000000ff
[0x17] ---                = 0xbbbbbbbb
[0x18] ---                = 0x0000175d
[0x19] ---                = 0x00000834
```

```
[0x1a] ---               = 0x00840121
[0x1b] ---               = 0x00840121
[0x1c] SEBP1             = 0x00009999
[0x1d] SEBP2             = 0x00099999
[0x1e] ---               = 0x00000000
[0x1f] ---               = 0x00840121
[0x20] DIVSET            = 0x0054f551
[0x21] ---               = 0x00000551
[0x22] ---               = 0x00840121
[0x23] ---               = 0x00840121
[0x24] SSCCTL            = 0x00010000
[0x25] ---               = 0x00840121
[0x26] ---               = 0x00840121
[0x27] ---               = 0x00000020
[0x28] ---               = 0x00640004
[0x29] PI12BiasParms     = 0x08880888
[0x2a] ---               = 0x08880888
[0x2b] ---               = 0x000087c0
[0x2c] ---               = 0x00000000
[0x2d] ---               = 0x00000000
[0x2e] ---               = 0x15780001
[0x2f] ---               = 0x00000001
[0x30] SSC1PARMS         = 0x1270a428
[0x31] SSC2PARMS         = 0x12704c30
[0x32] SSC3PARMS         = 0x12704c30
[0x33] SSC4PARMS         = 0x1270a428
[0x34] ---               = 0x00840121
[0x35] ---               = 0x00840121
[0x36] ---               = 0x00840121
[0x37] ---               = 0x00840121
[0x38] ---               = 0x00000000
[0x39] SSC2OCPARMS       = 0x00000000
[0x3a] ---               = 0x00000000
[0x3b] ---               = 0x00000000
[0x3c] ---               = 0x00840121
[0x3d] ---               = 0x00840121
[0x3e] ---               = 0x00840121
[0x3f] ---               = 0x00840121
[0x40] ---               = 0x29c529c5
[0x41] ---               = 0x29c529c5
[0x42] ---               = 0x00840121
[0x43] ---               = 0x00840121
[0x44] ---               = 0x00840121
[0x45] ---               = 0x00840121
[0x46] ---               = 0x00840121
[0x47] ---               = 0x00840121
[0x48] PMSRCCLK1         = 0x76543210
[0x49] PMSRCCLK2         = 0x00000f98
[0x4a] ---               = 0x00840121
[0x4b] ---               = 0x00840121
[0x4c] ---               = 0x00840121
[0x4d] ---               = 0x00000002
[0x4e] ---               = 0x00840121
[0x4f] ---               = 0x00000000
[0x50] ---               = 0x00840121
[0x51] ---               = 0x00840121
```

```
[0x52] ---                = 0x00840121

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.10 Example 10 - Read Register (Names)

```
C:\cct>cctwin.exe rr PLLEN OCKEN
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

[0x0c] PLLEN              = 0x6000000c
[0x0e] OCKEN              = 0x1fde078f

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.11 Example 11 - Read Register Dynamic

```
C:\cct>cctwin.exe rrd
Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

[0x20] DIVSET             = 0x0054f551[UNLOCKED]
[0x21] ---                = 0x00000551[UNLOCKED]
[0x24] SSCCTL             = 0x00010000[UNLOCKED]
[0x30] SSC1PARMS          = 0x1270a428[UNLOCKED]
[0x31] SSC2PARMS          = 0x12704c30[UNLOCKED]
[0x32] SSC3PARMS          = 0x12704c30[UNLOCKED]
[0x33] SSC4PARMS          = 0x1270a428[UNLOCKED]
[0x38] ---                = 0x00000000[UNLOCKED]
[0x39] SSC2OCPARMS        = 0x00000000[UNLOCKED]
[0x3a] ---                = 0x00000000[UNLOCKED]
[0x3b] ---                = 0x00000000[UNLOCKED]

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.12 Example 12 - Use SMR to Read Buffered Register

```
C:\cct>cctwin smr buffered divset

Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

[0x20] DIVSET             = 0x00355551

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.13 Example 13 - Use SMR to Read Register

```
C:\cct>cctwin smr divset

Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

[0x20] DIVSET             = 0x0054f551
```

```
HECI CMD Status = 0x00000000 (SUCCESS)
```

2.3.14 Example 14 - Use SMW to Write Register

```
C:\cct>cctwin smw divset=0

Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.


HECI CMD Status = 0x00000011 (REGISTER_IS_LOCKED)
```

2.3.15 Example 15 - Use GCEM to Get Currently used Clock Enables Mask Value

```
C:\cct>cctwin gcem

Intel (R) Clock Commander Tool Version: 8.0.0.xxxx
Copyright (C) 2010 Intel Corporation. All rights reserved.

Clock enables mask: before EOP = 0x00ff0f8f, after EOP = 0x00ff0f8f

HECI CMD Status = 0x00000000 (SUCCESS)
```

2.4 Error and Status Messages

2.4.1 Clock Commander Tool Error and Status Messages

When a command is executed the Clock Commander Tool will display status and error messages to indicate the result of the operations. The messages and their definitions are listed in the following table.

Table 2-1. CCT Error and Status Messages

CCT Message	Definition
SUCCESS	The command executed successfully.
FAILURE	The command failed to execute.
INVALID OPTION	An invalid option was specified for the command.
INVALID COMMAND	The command entered was invalid.
INVALID ARGUMENT	The argument entered was invalid.
REGISTER OFFSET OUT OF RANGE	The register offset entered was outside the allowable range.
TOO FEW ARGUMENTS	Arguments missing from the command.
HECI INITIALIZATION FAILED	Initialization of the Intel MEI interface failed.
HECI READ FAILED	A read from the Intel MEI interface failed.
HECI WRITE FAILED	A write to the Intel MEI interface failed.
SMBUS INITIALIZATION FAILED	Initialization of the SMBus failed.
MISSING SMBUS TRANSPORT LIBRARY (AARDVARK.DLL)	The Aardvark DLL is missing.

Table 2-1. CCT Error and Status Messages

CCT Message	Definition
SMBUS READ FAILED	A read from the SMBus failed.
SMBUS WRITE FAILED	A write to the SMBus failed.
INVALID OR NON EXISTENT SMBUS CONFIG FILE	There is an error in the cct.ini file or the file is missing.
INVALID RESPONSE	The command received an invalid response.
INVALID_FUNCTION	An invalid function was sent to the FW.
INVALID_PARAMS	A command failed due to invalid parameters.
FLASH_WEAR_OUT_VIOLATION	FW is indicating a flash wear out violation.
FLASH_CORRUPTION	FW is indicating that the flash is corrupted.
PROFILE_NOT_SELECTABLE_BY_BIOS	The ICC profile is not selectable by BIOS. It is selectable by a soft strap.
TOO_LARGE_PROFILE_INDEX	The profile sent by the command exceeds the number of profiles present in the flash.
NO_SUCH_PROFILE_IN_FLASH	The profile sent by the command does not exist in the flash.
CMD_NOT_SUPPORTED_AFTER_END_OF_POST	A command was attempted that is not allowed after end of post is received from the BIOS.
NO_SUCH_RECORD	A command attempted to access a non-existent record.
TOO_LARGE_REGISTER_INDEX	The register index is outside the allowable range.
TOO_LARGE_UOB_RECORD	A write UOB command failed because the UOB exceeded the allowable size.
REGISTER_IS_LOCKED	Access to the ICC register is denied because it is locked.
DOS_WAIT	The FW is currently in a denial of service wait state.
BAD_NONCE	A command was sent with an incorrect nonce.
DOS_WAIT_BAD_NONCE	The FW is currently in a denial of service wait because it received an incorrect nonce.
FUNCTION_NOT_SUPPORTED_AFTER_EOP_OVER_THIS_HECI	A command was attempted that is not allowed after end of post is received from the BIOS.
FUNCTION_NOT_SUPPORTED_OVER_SMBUS	A command is sent that is not supported over the SMBus.
DENIED_AUTO_LOCKED	Access to the ICC register is denied because they have been auto locked.
UOB_RECORD_IS_ALREADY_INVALID	This error occurs when CCT attempts to invalidate a UOB that is already invalid.
ONE_UOB_RECORD_IS_ALREADY_VALID	An attempt is made to create a UOB when one is already valid.
OCKEN_MASK_VIOLATION	An attempt is made to write to the OCKEN register that violates the clock enables mask settings.
SUCCESS_OCKEN_AUTO_LOCKED	The OCKEN register was successfully auto locked by FW.
RANGE_VIOLATION_FREQ_TOO_HIGH_CLK[x]	A command failed because the frequency exceeded the allowable range.

Table 2-1. CCT Error and Status Messages

CCT Message	Definition
RANGE_VIOLATION_FREQ_TOO_LOW_CLK[x]	A command failed because the frequency exceeded the allowable range.
SSC_MODE_CHANGE_NOT_SUPPORTED_CLK[x]	A command failed because a change to the spread spectrum mode is not supported for that clock.
AS EXPECTED, RESPONSE FROM ME FW NOT RECEIVED	No response from ME FW received

2.4.2 Boot Status

The Clock Commander Tool Command Get Clock Capabilities (gcc) returns an ICC boot status report which provided an indication of the status of integrated clock control after the system has booted. The possible results of the boot status are shown in the following table.

Table 2-2. ICC Boot Status Errors

Boot Status Message	Definition
IccBootRecoveryFailure	There was some failure during the ICC boot recovery.
RecoveredFromIccWdtTimeout	FW detected a watch dog timer expiration.
DisqualifiedIccProfile	The BIOS ICC profile was disqualified. This could be due to the FW not receiving the DRAM init done message.
IccProfileSelectionFailure	Selection of the ICC profile failed.
IccProfileIndexOutofRange	The selected ICC profile exceeds the number of profiles contained in flash.
OemPltParamsBlockInvalid	The ICC NVAR in flash has an invalid format.
IccCrdrCreationFailure	Creation of the clock range definition record failed.
OemClkRangeMinViolation	The OEM record violates one of the Intel minimum ranges.
OemClkRangeMaxViolation	The OEM record violates one of the Intel maximum ranges.
OemSprPrcntMaxViolation	The OEM record violates the Intel spread spectrum range for one of the clocks.
IntelRecordApplyingFailure	Application of the Intel record failed.
OemRecordViolatedClkRangeLimits	The OEM record violates the range limits for one of the clocks.
OemRecordApplyingFailure	Application of the OEM record failed.
PermUobViolatedClkRangeLimits	The permanent UOB is outside the clock ranges for one of the clocks.
PermUobApplyingFailure	Application of the permanent UOB failed.
SusramRecoveryFailure	FW was not able to successfully restore all the contents from SUSRAM to flash.
IntelCRDRSkuReducedEnhancedUpperRange	FW has detected that Intel ME clk OC might occur on Enhanced SKU and thus upper range for ME clk must be changed to basic.

Table 2-2. ICC Boot Status Errors

Boot Status Message	Definition
IntelCRDRSkuReducedExtremeRanges	FW has detected that Intel ME clk OC might occur on Extreme SKU and thus both ranges for Intel ME clk must be changed to basic.
OemRecordViolatedMEClkRestrictions	FW has detected that Intel ME clk is trying to be routed to CLK4 in the OEM Record.
UobRecordViolatedMEClkRestrictions	FW has detected that Intel ME clk is trying to be routed to CLK4 in the UOB Record.

Table 2-3. ICC Boot Status Informational Messages

Boot Status Message	Definition
GetIccProfileReceived	Get ICC profile command received.
SetClockEnablesReceived	Received set clock enables command from BIOS.
LockReceived	Received the lock ICC registers command from BIOS.
CmosBatteryRemoved	FW detected that the CMOS battery was removed.
InvalidatedUobRecord	The UOB record has been invalidated.